

CLAIMS

1. An image processing device in which a high-speed bus and a peripheral bus are linked via a bus bridge and in which connected to the high-speed bus and the peripheral bus are a CPU for carrying out computation and control of image processing, a data transceiving FIFO memory for carrying out transceiving of image compression data with a host device, a frame memory for storing image expansion data and displaying this data on a display panel, and a compression/expansion circuit for carrying out compression of image expansion data and expansion of image compression data,

wherein the CPU and the frame memory are connected to the high-speed bus and the data transceiving FIFO memory is connected to the peripheral bus.

2. The image processing device according to claim 1, wherein the compression/expansion circuit is connected to the high-speed bus.

3. An image processing device which has an CPU-direct instruction bus, a CPU-direct data bus, and a high-speed bus, and in which connected to these buses are a CPU for carrying out computation and control of image processing, a ROM for storing a processing program of the CPU, a RAM used as a work area for the computation carried out by the CPU, a data transceiving FIFO

memory for carrying out transceiving of image compression data with a host device, a frame memory for storing image expansion data and displaying this data on a display panel, and a compression/expansion circuit for carrying out compression of image expansion data and expansion of image compression data,

wherein the CPU and the ROM are connected to the CPU-direct instruction bus, the CPU, the RAM, and the frame memory are connected to the CPU-direct data bus, and the CPU and the data transceiving FIFO memory are connected to the high-speed bus.

4. The image processing device according to claim 3,

wherein the compression/expansion circuit is connected to the CPU-direct data bus.